International Journal of Electronics and Communication Engineering (IJECE)
ISSN 2278-9901
Vol. 2, Issue 3, July 2013, 91-96

International Academy of Science, Engineering and Technology
Connecting Researchers; Nurturing Innovations

IMPLEMENTATION OF REVERSIBLE GATES AND IT'S APPLICATION

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ABSTRACT

Reversible logic has become one of the most promising technologies in the recent past, with applications in several fields; such as low power CMOS, nanocomputing and optical computing etc. This paper presents reversible gates and reversible logic implementations for Binary Coded Decimal (BCD) adder. Reversible logic gates are widely known to be compatible with future computing technologies which virtually dissipate zero heat. The main virtue of BCD adders is that it allows easy conversion to decimal digits for printing or display and faster decimal calculations. These reversible BCD circuits are basis of the decimal ALU of primitive Quantum CPU. The proposed BCD adders have been simulated in VLSI.

KEYWORDS: Reversible Logic, BCD Adder, VLSI, Zero Heat Dissipation

INTRODUCTION

The quest for better and smaller computing circuits has fuelled modern advances in fabrication technology for logic circuits which has consequently resulted in improved performance and led to optimal performance of logic devices. Further improvements were limited earlier, by the Landauer principle, which stated that information loss led to heat dissipation. Each bit of information lost generates kTln2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed However, it was Bennett who proved that using a network consisting of reversible gates, the energy dissipation can be neutralized.

Bennett showed that kTln2 energy dissipation would not occur if the computation were carried out in a reversible manner, since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system consists of reversible gates.Reversible logic has also found several applications in quantum computing, nanotechnology, DNA technology and optical computing.

In this paper, improved design techniques of reversible gates and reversible logic implementation for BCD adder is presented.Faster hardware for decimal floating-point arithmetic is also imminent as it has its importance in financial, Internet based applications. So, faster circuits for Binary Coded Decimal (BCD) numbers have great impact. Also incorporated in more complex circuits like future Mathematical processors.

BASIC DEFINITIONS

Reversible Gates: Reversible gates are logical circuits which have same number of inputs and outputs and there is a one to one correspondence between the vector of inputs and outputs.

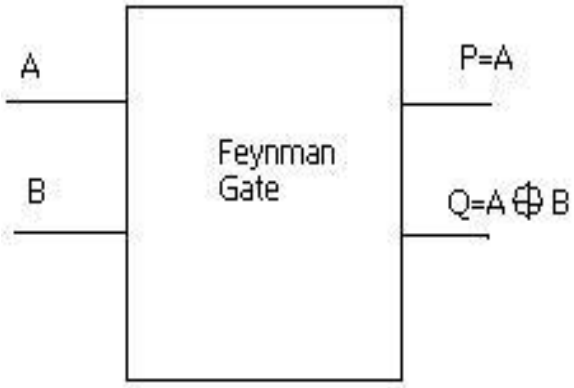

Figure 1: Feynman Gate (Two Input and Two Output)

Garbage Output: Garbage outputs are the unutilised outputs required to maintain reversibility.

Necessary condition for reversibility is that the gate has the same number of input and output.

REVERSIBLE GATES AND PROPOSED DESIGN OVERVIEW

The newly proposed reversible gates, utilized in designing the proposed reversible BCD adder.

Peres Gate

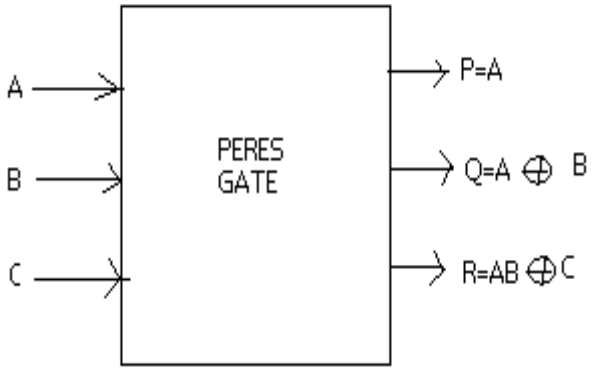

Figure 2: Peres Gate 3*3

In Peres gate, it can be verified that input pattern corresponding to output pattern can be uniquely determined.

Table 1: Truth Table for Peres Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

DESIGN PROPOSED FOR BCD ADDER

Reversible BCD Adders Have Used the Following

The circuit consists of a parallel adder, a combinational part and another parallel adder which is used for error correction. In the first 4-bit parallel adder, initial sum is produced by binary summation of two BCD numbers. In the combinational part, BCD overflow is detected. In the correction part, a 4 bit parallel adder is used to add the error correction value whenever an overflow occurs.

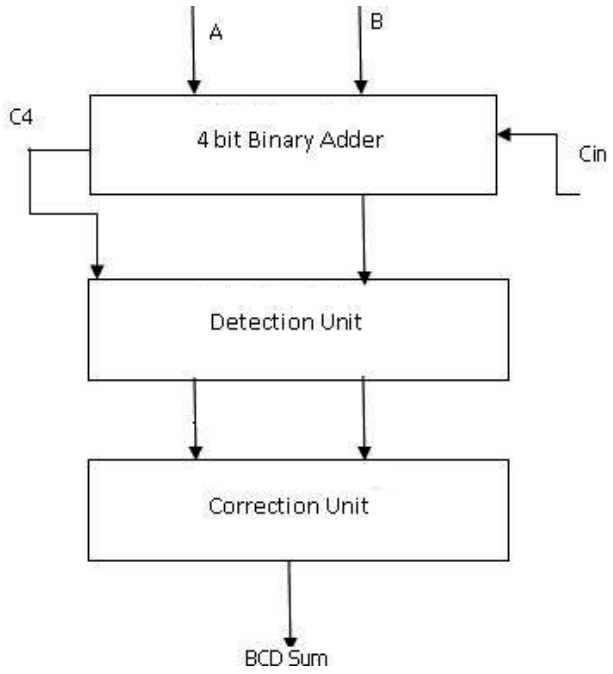

Figure 3: BCD Addition Design Structure

PROPOSED DESIGN OF REVERSIBLE BCD ADDER

This section will detail the improved designs for reversible BCD adder.

Background on BCD adders:-A full-adder is a device that takes as input two input bits and a carry-in bit and produces as output the sum of the bits and the carry-out. A reversible full adder can be realized by at least one gate. However, a reversible 4-bit parallel adder needs at least 4 reversible gates. A combinational circuit for BCD overflow detection is a circuit that checks whether the result of the binary addition of the two BCD number overflows. The error correction unit add the error correction value whenever an overflow occurs.

Proposed BCD Adder Design

A reversible BCD adder consists of three components: a 4-bit parallel adder, BCD adder overflow detection logic and BCD adder overflow correction logic.

In this section, Designs for Reversible BCD adder have been presented with detail algorithms and figures.

Adder: A full-adder is a device that takes as input two input bits and a carry-in bit and produces as output the sum of the bits and the carry-out.A reversible full adder can be realized by at least one gate respectively. A reversible 4-bit parallel adder can be realized by at least 4 reversible gates that prove that a reversible full adder can be realized by at least one gate. As a reversible 4-bit parallel adder consists of 4 reversible full adders, a reversible 4-bit parallel adder can be realized by at least 4 x 1 = 4 gates.

Overflow Detection: A combinational circuit for BCD overflow detection is a circuit that checks whether the result of the binary addition of the two BCD numbers overflows. A BCD number overflow occurs if the resulting number is greater than 1001(decimal 9). Let A3A2A1A0 and B3B2B1B0 be the two BCD numbers to be added and the resulting number is represented by T3T2T1T0. Carry out is represented by C4. C4 is set when the resulting number is greater than 1111, i.e. decimal 15. Six invalid BCD numbers can be detected by the condition (T2+T1). T3. So, the expression for overflow detection bit, F is (T2+T1). T3 + C4. However, it is easy to note that (T2+T1). T3 and C4 cannot be set at the same time. If F is set, an overflow has been occurred.

Error Correction: In error correction logic, 0110 (decimal 6) is added to the partial sum, T3T2T1T0 and any carry out from this addition is ignored. Carry out from the addition of two BCD numbers A3A2A1A0 and B3B2B1B0 is already computed along with F. If F is not set, no error correction is needed. The partial sum, T3T2T1T0 itself becomes the final result.

In order to propose the 1-digit BCD adder, have proposed three Unit. Algorithm I, termed as **Overflow_Detection (ODA),** is used to detect the overflow produced by adding two BCD digits. **Overflow_Correction_Algorithm (OCA)**, or Algorithm II, is used to correct the error generated by adding two BCD digits. Finally, Algorithm III, which is termed as **BCD Adder Construction Algorithm**, is used to design the overall circuit.

ALGORITHM I:-OVERFLOW DETECTION ALGORITHM (ODA)

Overflow detection bit, F = (T2+T1). T3. C4. The expression shows that the resulting circuit may contain at least two blocks. The approach might be similar to the following

Begin

Step 1: The first block will take T1 and T2 and output (T2+T1).

Step 2: The second block will take the T3, C4 and output from first block (T2+T1) and compute the

Result F = (T2+T1). T3. C4.

Return R: = T . F;

End

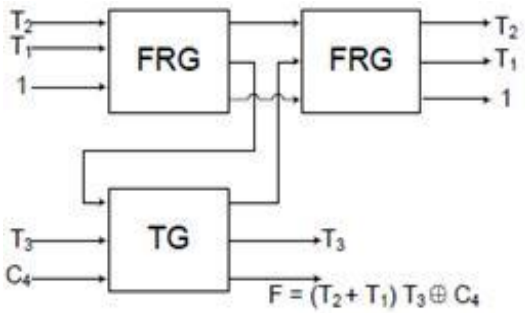

Figure 4: Overflow Detection Algorithm

ALGORITHM II:-OVERFLOW CORRECTION ALGORITHM (OCA)

Begin

Step 1: The first block will take T1 and F from the overflow detection logic circuit. Generate S1 = T1. F and carry_out1 = T1.F.

Step 2: The second block will take carry out of the first block, T2 from the overflow detection Circuit and F and generate S2 = T2. F. carry_out1. It will also generate carry_out2 = (T2. F). carry_out1+ T2.F.

Step 3: The third block will take carry out of the second block, T3 from the overflow detection

Circuit and generate S3 = T3. carry_out2.

Return S;

End

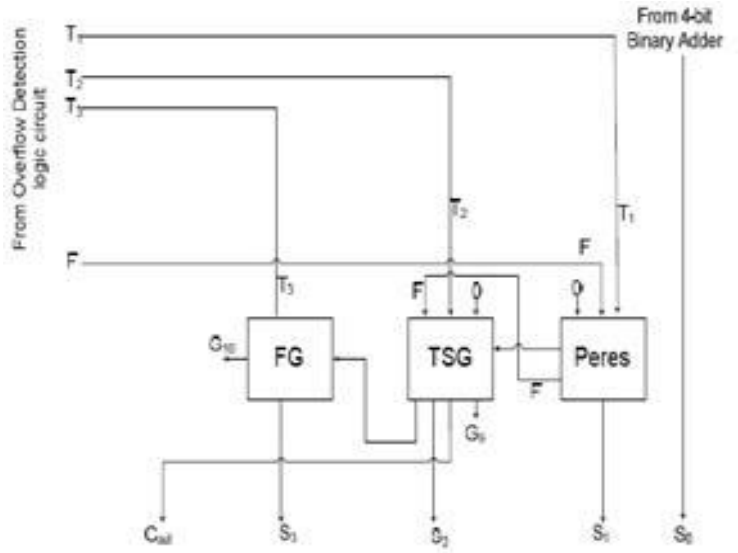

Figure 5: Overflow Correction Algorithm

ALGORITHM III:-BCD ADDER ALGORITHM

Combining all the algorithms together to calculated BCD addition. Given Input: A = (A3, A2, A1, A0) and B= (B3, B2, B1, B0) are two 4-bit input BCD vectors.

Input: A = (A3, A2, A1, A0) and B= (B3, B2, B1, B0) are two 4-bit input BCD vectors.

Output: Final corrected BCD sum S (Cout, S3, S2, S1, and S0).

Begin

T: = Binary Adder output (A, B);

R: = ODA (T);

S: = OCA(R);

Return S;

End

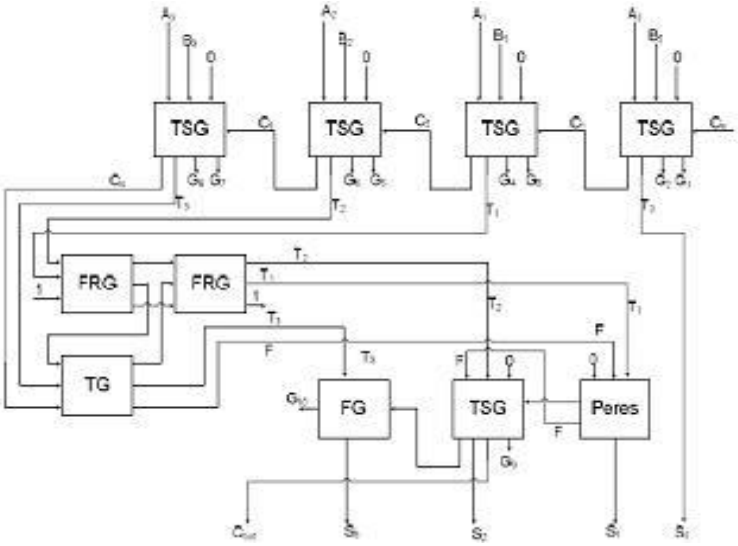

Figure 6: Design of a 1-Digit BCD Adder

RESULTS

In this paper, reversible logic synthesis carried out for BCD adder. The designs have been done for ease of reversible logic implementation and it has been found that the proposed designs are far better than the existing in terms of number of gates needed, number of garbage outputs produced and delay. Improved BCD adder can perform much faster than the BCD adder.Fast and improved BCD adders may also find its use in future quantum computers.

CONCLUSIONS

The BCD Adder simulation is done using TANNER tool. It is proved that proposed design reduce the power dissipation in reversible circuits. In BCD Adder instead of using existing full adder using TSG gate, replace it by Peres full adder to reduce the garbage counts and power dissipation. This can be further extended for design of different types of reversible gates and also to use these gates for various applications.

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